PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Simon DELEONIBUS

Application No.: New U.S. Patent Application

Filed: September 6, 2006 Docket No.: 129344

For: FIELD EFFECT TRANSISTOR WITH SUITABLE SOURCE, DRAIN AND CHANNEL MATERIALS AND INTEGRATED CIRCUIT COMPRISING SAME

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 CFR §1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

☒ 1. This Information Disclosure Statement is being filed (a) within three months of the U.S. filing date of this non-CPA application, OR (b) before the mailing date of a first Office Action on the merits in the present application. No certification or fee is required.

☒ 2. Relevance of one or more non-English language reference is discussed in the present specification. See References 4 and 5.

☒ 3. One or more reference cited herein was cited in the International Search Report. An English language version of the International Search Report is attached for the Examiner's information. See References 1 - 9.

☒ 4. In accordance with 37 CFR §1.98(a)(2)(ii), copies of any U.S. patents and patent application publications are not attached.

☒ 5. An English language Abstract of one or more non-English language reference is attached hereto. See References 4 - 7.

Respectfully submitted,

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WPB:DAT/kam

Date: September 6, 2006

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DEPOSIT ACCOUNT USE AUTHORIZATION
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Form PTO-1449 (REV. 1/06)	US Dept. of Commerce PATENT & TRADEMARK OFFICE	ATTY DOCKET NO. 129344	APPLICATION NO. New U.S. Patent Application
INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)		APPLICANT(S) Simon DELEONIBUS	
		FILING DATE September 6, 2006	

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Name
	1	2004/0014276	01/22/2004	MURTHY et al.
	2	2001/0020725 A1	09/13/2001	OKUNO et al.
	3	6,187,641 B1	02/13/2001	RODDER et al.

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number	Date	Country	With English Abstract	With English Translation
	4	JP A 63-122177	05/26/1988	JAPAN	X	
	5	JP A 63-013379	01/20/1988	JAPAN	X	
	6	JP A 01-112772	05/01/1989	JAPAN	X	
	7	JP A 61-276265	12/06/1986	JAPAN	X	

OTHER DOCUMENTS

Examiner Initials	Cite No.	(Including Author, Title, Date, Pertinent Pages, etc.)
	8	Subramanian, V., et al. "A Novel Technique for 3-D Integration: Ge-seeded Laterally Crystallized TFTs." *1997 Symposium on VLSI Technology -- Digest of Technical Papers*, pp. 97 - 98, June 10, 1997.
	9	Lindert, N. et al. "Quasi-Planar FinFETs with Selectively Grown Germanium Raised Source/ Drain." *2001 International SOI Conference Proceedings*, pp. 111-112, October 1, 2001.

EXAMINER	DATE CONSIDERED

Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date: September 6, 2006